151. (Amended) A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells and a programmable register, the method of operation of the memory device comprises:

sampling a first operation code synchronously with respect to a transition of an external clock signal;

receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, wherein the second operation code specifies a read operation to the memory device; and

storing the binary value in the programmable register in response to the first operation code.

152. The method of claim 151 wherein the first operation code is included in a control register access request packet.

153. The method of claim 152 wherein the first operation code and the binary value are included in the same control register access request packet.

154. The method of claim 151 wherein the delay time is representative of a number of clock cycles of the external clock signal.

155. The method of claim 154 further including:

receiving the second operation code; and

outputting the data, in response to the second operation code, after the number of clock cycles of the external clock signal transpire.

156. The method of claim 155 further including sampling address information synchronously with respect to the external clock signal.

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157. The method of claim 156 wherein the address information and the second operation code are included in a read request packet.

8 158. (Twice Amended) The method of claim 151 further including:

receiving block size information, wherein the block size information is representative of an amount of data to be output;

receiving the second operation code; and

outputting the amount of data, in response to the second operation code, after the delay time transpires.

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159. (Amended) The method of claim 158 wherein the block size information further defines an amount of data to be input in response to a third operation code, wherein the third operation code specifies a write operation to the memory device, the method further including:

receiving the third operation code; and

inputting the amount of data in response to the third operation code.

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160. The method of claim 159 wherein the third operation code is included in a write request packet.

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161. The method of claim 160 wherein the block size information and the third operation code are included in the same write request packet.

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162. (Amended) The method of claim 151 further including:

receiving the second operation code; and

outputting data in response to the second operation code, wherein the data is output synchronously with respect to consecutive rising and falling edge transitions of the external clock signal.

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163. (Amended) The method of claim 151 wherein the first operation code is received during an initialization sequence after power is applied to the memory device.

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164. (Twice Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code specifies an access of the programmable register in the memory device in order to store a binary value, wherein the binary value is representative of control information; and

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

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165. The method of claim 164 wherein the control information is representative of a number of clock cycles of an external clock signal to transpire before the memory device outputs data in response to a second operation code.

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166. The method of claim 165 further including:

issuing the second operation code to the memory device; and

receiving data output by the memory device after the number of clock cycles of the external clock signal transpire.

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167. The method of claim 166 further including providing address information to the memory device synchronously with respect to the external clock signal.

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168. The method of claim 167 wherein the address information and the second operation code are included in a request packet.

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169. The method of claim 164 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device in response to a second operation code;

issuing the second operation code to the memory device; and

receiving the amount of data output by the memory device.

Cont. E1

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170. The method of claim 169 wherein the block size information further defines an amount of data to be input by the memory device in response to a third operation code, the method further including:

issuing the third operation code to the memory device; and

providing the amount of data to the memory device.

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171. The method of claim 164 wherein the first operation code and the binary value are included in a request packet.

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172. (Amended) The method of claim 171 wherein the first operation code and the binary value are included in the same request packet.

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173. A synchronous memory device including an array of memory cells, the synchronous memory device comprising:

a clock receiver to receive an external clock signal;

a plurality of input receivers to sample a first operation code synchronously with respect to a transition of the external clock signal; and

a programmable register to store a binary value that is representative of control information, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

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174. (Twice Amended) The memory device of claim 173 wherein the control information is representative of a number of clock

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cycles of the external clock signal to transpire before the memory device outputs data, and wherein the memory device outputs the data in response to a second operation code.

33 ~~175~~. The memory device of claim ~~174~~ further including a plurality of output drivers to output the data, after the number of clock cycles of the external clock signal transpire, in response to the second operation code.

~~176~~. (Thrice Amended) The memory device of claim ~~173~~ further including a plurality of output drivers to output data in response to a second operation code, wherein the second operation code specifies a read operation, and wherein the plurality of output drivers output a first portion of the data synchronously with respect to a rising edge transition of the external clock signal and output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

~~177~~. The memory device of claim ~~173~~ wherein the first operation code is included in a request packet.

~~178~~. (Amended) The memory device of claim ~~173~~ wherein the first operation code and the binary value are each included in a request packet.

~~179~~. The memory device of claim ~~178~~ wherein the first operation code and the binary value are included in the same request packet.

~~180~~. (Twice Amended) The memory device of claim ~~173~~ wherein the plurality of input receivers are operative to receive a second operation code, wherein the second operation code specifies a write operation to the memory device, and wherein the memory device

further includes additional input receivers to input data in response to the second operation code.

181. The method of claim 151 wherein the first operation code is sampled from an external bus.

182. The method of claim 181 wherein the external bus includes a plurality of signal lines, and wherein the binary value and the first operation code are multiplexed over the plurality of signal lines.

183. The method of claim 164 wherein the first operation code is issued to the memory device via an external bus.

184. The method of claim 183 wherein the external bus includes a plurality of signal lines, and wherein the binary value and the first operation code are multiplexed over the plurality of signal lines.

185. The memory device of claim 173 wherein the array of memory cells includes dynamic random access memory cells.

186. The memory device of claim 173 wherein the plurality of input receivers sample the first operation code from an external bus.

187. The memory device of claim 186 wherein the external bus includes a plurality of signal lines, and wherein the first operation code and the binary value are multiplexed over the plurality of signal lines.

188. The memory device of claim 187 wherein data, the first operation code and the binary value are multiplexed over the plurality of signal lines.

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189. The memory device of claim 173 further including a delay locked loop, coupled to the clock receiver, to generate an internal clock signal using the external clock signal.

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190. The memory device of claim 189 further including a plurality of output drivers, coupled to the delay locked loop, to output data in response to the internal clock signal, wherein the data is accessed from the memory array.

Cont. E1

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191. The memory device of claim 190 wherein the plurality of output drivers output a first portion of the data synchronously with respect to a rising edge transition of the external clock signal, and wherein the plurality of output drivers output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

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192. (Amended) The memory device of claim 191 wherein the programmable register is included in a plurality of programmable registers of the memory device, each register of the plurality of registers to store a corresponding binary value.

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193. The method of claim 164 wherein the control information includes a device type identifier.

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194. The method of claim 164 wherein the control information identifies a location of a defective portion of the array of memory cells.

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195. The method of claim 164 wherein the control information identifies a range of addressable locations of the array of memory cells.

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196. The method of claim 164 wherein the control information

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includes a device identification value to identify the memory device uniquely among a plurality of memory devices.

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~~197~~. The memory device of claim ~~173~~ wherein the control information includes a device identifier.

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~~198~~. The memory device of claim ~~173~~ wherein the control information identifies a location of a defective portion of the array of memory cells.

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~~199~~. The memory device of claim ~~173~~ wherein the control information identifies a range of addressable locations of the array of memory cells.

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~~200~~. The memory device of claim ~~173~~ wherein the control information includes a device identification value to identify the memory device uniquely among a plurality of memory devices.

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~~201~~. The memory device of claim ~~173~~ further including a plurality of registers, wherein the programmable register is included in the plurality of registers, and wherein the plurality of registers further includes at least one of:

a first register to store a value that identifies the memory device uniquely among a plurality of memory devices;

a second register to store a value that identifies a range of addressable locations of the array of memory cells; and

a third register to store a value that identifies a location of a defective portion of the array of memory cells.

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